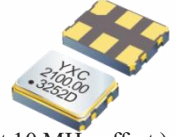


Differential Oscillator

YSO231LJ



Applications

- 10 GB Ethernet,
SONET, SATA, SAS,
Fibre Channel

Features

- Femto second integrated phase jitter
(50fs typical, 12KHz to 20 MHz)
- Output LVPECL, HCSL or LVDS.

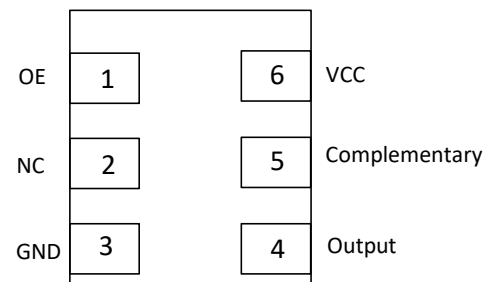
- Superior phase noise
(-157 dBc/Hz at 100 KHz and -164 dBc/Hz at 10 MHz offset)
- Package Size: 2.5*2.0 , 3.2*2.5 , 5.0*3.2
7.0*5.0mm

Specifications (规格参数)

Item/Type	LVPECL	LVDS	HCSL				
Output Frequency Range	100~250MHZ	100~250MHZ	100~175MHZ				
Supply Voltage	2.5V, 3.3V	1.8V, 2.5V, 3.3V	1.8V, 2.5V, 3.3V				
Operating Temperature Range	-40~+85°C, or specify						
Storage Temperature Range	-55~+150°C						
Total Stability	±25ppm, ±50ppm, ±100ppm or specify						
Current Consumption	52mA(Typ) 65mA(Max)	22mA(Typ) 30mA(Max)	32mA(Typ) 40mA(Max)				
Output Swing (single-end)	400 mV (min.)	200 mV (min.)	450 mV (min.)				
Output Load Condition	50 Ω into VDD - 2.0V or Thevenin equivalent	100 Ω between output and complimentary output	50 Ω to ground on each output				
Duty Cycle	45~55%						
Rise Time/Fall Time(20%↔80% of waveform)	0.15ns(Typ) 0.4ns(Max)	0.15ns(Typ) 0.3ns(Max)	0.2ns(Typ) 0.6ns(Max)				
Start-up time	1ms(Typ) 5ms(Max)						
Aging at Ta = +25°C	± 3 ppm (max.) first year ; ± 2 ppm (max.) per year thereafter						
RMS Jitter (12 KHz to 20 MHz)	50 fsec (typ.) , 300 fsec (max.) [For 125 MHz , LVDS , 3.3V]						
Phase Noise[dBc / Hz (typ.)]	Offset	100Hz	1KHz	10KHz	100KHz	1MHz	10MHz
	125.0MHz	-114	-135	-147	-157	-163	-164
	156.250MHz	-108	-132	-141	-152	-160	-161
Output Enable / Disable Function	Enable	70% (min.) of VDD to enable output. Enable time : 10 msec (max.)					
	Disable	70% (min.) of VDD to enable output. Enable time : 10 msec (max.)					

Pin Dimension (脚位尺寸)

Pin	#1	#2	#3
FUNCTION	OE	No Connection	Ground
Pin	#4	#5	#6
FUNCTION	Output	Complementary	Supply Voltage



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Dimensions and Recommended land pattern (外观尺寸及推荐焊盘)

Package Size – Dimensions (Unit: mm)	Recommended Land Pattern (Unit: mm)
<p>2.5*2.0mm</p> <p>Top view</p> <p>Bottom view</p> <p>Side view</p>	
<p>3.2*2.5mm</p> <p>Top view</p> <p>Bottom view</p> <p>Side view</p>	
<p>5.0*3.2mm</p> <p>Top view</p> <p>Bottom view</p> <p>Side view</p>	
<p>7.0*5.0mm</p> <p>Top view</p> <p>Bottom view</p> <p>Side view</p>	

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Test Circuit (测试电路)

